REMARKS

Entry of the above amendment and reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-5 and 21-22 are pending in this case. Claims 1 and 21 are amended herein and claim 6 is cancelled herein. Claim 22 is added herein to more completely cover that which Applicant regards as the invention.

The Examiner rejected claims 1-6 and 21 under 35 U.S.C.§ 103(a) as being unpatentable over Uchiyama et al. (U.S. Patent 6,831,313) in view of Fox et al. (U.S. Patent 6,627,930).

Applicant respectfully submits that amended claim 1 is patentable over Uchiyama in view of Fox as there is no disclosure or suggestion in the references of capacitor stacks each having an upper electrode, a lower electrode, and a single ferroelectric core layer, wherein at least one of the capacitor stacks comprises a conductive contact formed thereunder and wherein the conductive contact has a cross section near a contact portion with the bottom portion of the stack that is about as large or larger than that of the ferroelectric cores. Uchiyama teaches a capacitor stack including an upper electrode 126, lower electrode 122 with barrier 121 and ferroelectric core 124. Uchiyama further teaches a conductive contact 120 under the capacitor stack. However, contact 120 does not have a cross-section near a contact portion with the bottom portion of the stack that is about as large or larger than that of the ferroelectric cores (see, Fig. 5). Fox is not applied to teach the underlying conductive contact. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are patentable over the references.

Applicant respectfully submits that dependent claim 21 is further patentable over the references. Claim 21 further requires an additional conductive contact over the ferroelectric core and upper electrode having a cross section about as large or larger than that of the ferroelectric cores and extending through the dielectric layer to a metal interconnect layer. Uchiyama teaches a metal interconnect formed on the top electrode rather than a conductive contact that extends to a metal interconnect. Element 126 of Uchiyama is an upper electrode of the capacitor stack. There is no suggestion of conductive contact overlying an upper electrode of the capacitor stack. Accordingly, Applicant respectfully submits that claim 21 is further patentable over the references.

Applicant respectfully submits that newly added claim 22 is patentable over the references as there is no disclosure or suggestion in the references of an array of ferroelectric memory cells, each cell having a capacitor stack comprising a lower barrier layer, a lower electrode, a single ferroelectric core layer, an upper electrode and an upper barrier, wherein at least one of the capacitor stacks comprises a conductive contact formed thereover and thereunder, and wherein the conductive contact has a cross section near a contact portion with the top portion of the stack and the bottom portion of the stack that is about as large or larger than that of the ferroelectric cores. Uchiyama teach a capacitor stack comprising a lower barrier layer 121, lower electrode 112, ferroelectric core 124, and an upper electrode 126. Uchiyama further teaches an underlying contact 120 having a cross-section smaller that the ferroelectric core rather than as large or larger as claimed. Uchiyama does not teach both an upper barrier layer and conductive contact formed thereover. Accordingly, Applicant respectfully submits that claim 22 is patentable over the references.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-5 and 21-22. If the Examiner has any questions or

Appl. No. 10/749,668 Reply to Office action of 07/13/2007

other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

/Jacqueline J Garner/

Jacqueline J. Garner Reg. No. 36,144

Texas Instruments Incorporated P. O. Box 655474, M.S. 3999 Dallas, Texas 75265 Phone: (214) 532-9348

Fax: (972) 917-4418